ABSTRACT OF THE DISCLOSURE

The semiconductor memory system includes a memory controller, *N* system data buses, and first through *P*-th memory module groups. The *N* system data buses are connected to the memory controller and respectively have a width of *M*/*N* bits. The first through *P*-th memory module groups are connected to the *N* system data buses and respectively have *N* memory modules. In each of the first through *P*-th memory module groups, a different one of the *N* system data buses is connected to each of the *N* memory modules, and each of the *N* system data buses has a data bus width of *M*/*N* bits. The first through *P*-th memory module groups are operated in response to first through *P*-th corresponding chip select signals. *M* is the bit-width of an entire system data bus of the semiconductor memory system. The *N* system data buses are wired such that data transmission times are the same from each *N* memory modules that operate in response to the same chip select signal to the memory controller.